

## Patent Claims

1. A quantizer (2) for a sigma delta modulator (1) comprising at least one preliminary stage (V1, V2), the quantizer (2) quantizing an input signal ( $E_Q$ ) present at it in accordance with at least one threshold signal ( $y_{th,i}$ ) and outputting it as a result value ( $y_Q$ ) at a digital result output (OUT), wherein the quantizer (2) has a number of comparators ( $5_j$ ) corresponding to the number ( $j$ ) of threshold signals ( $y_{th,j}$ ), which compare the input signal ( $E_Q$ ) with the respective threshold signal ( $y_{th,j}$ ), the threshold signal being reduced or increased by a correction voltage ( $y_{dac3}$ ) or a correction current, the correction voltage or correction current being generated in accordance with the result value ( $y_Q$ ) output at the result output (OUT).
2. The quantizer as claimed in Claim 1, wherein a number of comparators ( $5_i$ ,  $6_1$ ) corresponding to the resolution of the quantizer (2) is provided, the comparators having uniformly graduated threshold voltages ( $V_{th,i}$ ) or threshold currents.
3. The quantizer as claimed in Claim 2, wherein the quantizer (2) has a number of voltage comparators ( $6_1$ ) corresponding to the number of its resolution intervals, the voltage comparators comparing the input signal (21) present as input signal voltage ( $6_2$ ) with an associated threshold signal voltage ( $6_{3_i}$ ) and, if the input signal voltage exceeds or drops below the threshold signal voltage, outputting a corresponding digital result bit (0/1) ( $Q_i$ ), a digital adder ( $6_6$ ) being provided which adds the digital result value (22) of the last weighting of the comparators of the quantizer (1) to the individual threshold signal voltages of the comparators by increasing or reducing the

threshold signal voltages by part voltages (25) corresponding to the digital result value.

4. The quantizer as claimed in Claim 3, wherein a  
5 reference voltage generator (65) is provided which generates the threshold signal voltages ( $63_i$ ), which are different for each voltage comparator (61), the threshold signal voltages being selectable in part voltages (25), the threshold  
10 signals exhibiting, in particular, fixed differences with respect to one another.
5. The quantizer as claimed in one of Claims 1 to 16,  
15 wherein the adder (66) is associated with a switching mechanism which has switches (67) at the inputs of which the part voltages (25) of the reference voltage generator (65) are present and the outputs of which are connected to the inputs ( $V_{th_i}$ ) for the threshold signal voltages ( $63_i$ ) of  
20 the comparators (61), the switches being controlled by the output signal (Add<0:6>) of the adder.
6. A sigma delta modulator (1) comprising a quantizer  
25 (2) as claimed in one of Claims 1 to 5.
7. A sigma delta modulator (1) comprising a signal  
input (IN) at which an evaluation signal (x) to be evaluated is present, and a digital result output  
30 (OUT) which outputs a digital result value ( $y_Q$ ), a quantizer (2) being provided which quantizes an input signal ( $E_Q$ ) present at it in accordance with at least one threshold voltage ( $y_{th,i}$ ) and outputs it as a result value ( $y_Q$ ) at the digital result  
35 output (OUT),  
the quantizer (2) being preceded at its input by at least one preliminary stage ( $V_i$ ), which comprises an adder ( $3_i$ ), processing a preliminary stage input signal ( $E_i$ ) with an integrator ( $4_i$ )

following the adder in the signal path and supplying a preliminary stage output signal ( $A_i$ ), the adder ( $3_i$ ) being supplied with a feedback signal ( $R_i$ ), generated in dependence on the result value ( $y_Q$ ) for addition to the preliminary stage input signal ( $E_i$ ),  
5 the evaluation signal ( $x$ ) being present as preliminary stage input signal ( $E_1$ ) at a first preliminary stage ( $V_1$ ) and the preliminary stage output signal ( $A_{n-1}$ ) of the in each case previous preliminary stage ( $V_{n-1}$ ) in the signal path being present as preliminary stage input signal ( $E_n$ ) at each further preliminary stage ( $V_n$ ), the last preliminary stage ( $V_m$ ) before the quantizer (2)  
10 supplying the input signal ( $E_Q$ ) to the quantizer as preliminary stage output signal ( $A_m$ ), wherein the quantizer (2) exhibits a number of comparators ( $5_j$ ) corresponding to the number ( $j$ ) of threshold voltages ( $y_{th,j}$ ), which compare the input signal ( $E_Q$ ) with the respective threshold voltage ( $y_{th,j}$ ), the threshold voltage being reduced or increased by a correction voltage ( $y_{dac3}$ ), the correction voltage being generated in accordance with the result value ( $y_Q$ ) output at  
15 the result output (OUT).  
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8. The sigma delta modulator as claimed in Claim 7, wherein a digital/analog converter (6) is provided which generates an analog rough signal (RS) from  
30 the digital result value ( $y_Q$ ).

9. The sigma delta modulator as claimed in Claim 8, wherein the rough signal (RS) is in each case multiplied by a predetermined factor ( $b_i$ ) to the  
35 respective feedback signal ( $R_i$ ) of a preliminary stage ( $V_i$ ) corresponding to the position ( $i$ ) and the number of preliminary stages ( $V_i$ ) in the signal path.

10. The sigma delta modulator as claimed in one of Claims 7 to 9, wherein the correction voltage ( $y_{dac3}$ ) is a voltage corresponding to the result value ( $y_0$ ) multiplied by a fixed factor ( $b_3$ ).  
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11. The sigma delta modulator as claimed in Claim 10, wherein the factor ( $b_3$ ) is a simple fraction.
- 10 12. The sigma delta modulator as claimed in one of the preceding claims, wherein a digital/analog converter (6) is provided which generates the voltage corresponding to the result value.
- 15 13. The sigma delta modulator as claimed in one of the preceding claims, wherein a digital adder (7) is provided which adds the factor ( $b_3$ ) to the result value ( $y_0$ ) and connects a previously generated threshold voltage ( $y_{th,i}$ ), corresponding to the result, to the comparators ( $5_i$ ).  
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14. The sigma delta modulator as claimed in one of the preceding claims, wherein the sigma delta modulator is of second order with two preliminary stages.  
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15. The sigma delta modulator as claimed in one of the preceding claims, wherein the sigma delta modulator is a continuous-time sigma delta modulator.  
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16. The sigma delta modulator as claimed in one of the preceding claims, wherein a device (8) for editing the output signals of the adder ( $3_i$ ) is provided.
- 35 17. The sigma delta modulator as claimed in one of the preceding claims, wherein a number of comparators ( $5_i$ ) corresponding to the resolution of the quantizer (2) is provided, the comparators exhibiting uniformly graduated threshold voltages.

- 5 18. The sigma delta modulator as claimed in one of the preceding claims, wherein a reference voltage generator (9) is provided which supplies part voltages, from which the threshold voltages ( $y_{th,i}$ ) are generated.